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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/475,879	12/30/99	LACEY T	0325.00292

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EXAMINER	
TRAN, A	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 10/11/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/475,879	LACEY ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1, 6-15, 17, and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by McClintock et al (6,271,679 B1).

Regarding claim 1, McClintock shows a programmable logic device (Fig. 2, 4, 5, & 9) comprising:

One or more horizontal routing channels (GH, Fig. 5);

One or more vertical routing channels (GV);

One or more logic elements (a logic element including 16 LABs and 16 local interconnects, col. 5, lines 56-59) each configured to connect between one of the horizontal routing channels and one of the vertical routing channels, wherein each of the logic elements comprises (i) a logic block array (one LAB including 5 blocks, two LEs is considered one block), and (ii) an interconnect matrix (MegaLLAB, col. 5, lines 60-65) coupled to the logic block array, the horizontal routing channel and the vertical routing channel; and

A memory block (ESB, col. 6, lines 4-7) coupled to either (a) the interconnect matrix or (b) the horizontal routing channel and the vertical routing channel.

Regarding claim 6, McClintock shows the memory block is coupled to the interconnect matrix.

Regarding claim 7, McClintock shows a plurality of I/O blocks (IOE), wherein each I/O block of the plurality of I/O blocks is connected to a different end of the horizontal and the vertical routing channels.

Regarding claim 8, McClintock shows the I/O blocks are grouped into I/O banks (Fig 8).

Regarding claim 9, McClintock shows the I/O blocks comprise configurable I/O cells (Fig. 9).

Regarding claim 10, McClintock shows one or more dedicated inputs for I/O cell control (4 dedicated inputs, Fig. 9).

Regarding claim 11, McClintock shows one or more dedicated clock inputs (2 dedicated clock inputs).

Regarding claim 13, McClintock shows the dedicated inputs for I/O control comprises a reset input (at CLRN, Input Register).

Regarding claim 14, McClintock shows the dedicated inputs for I/O control comprises an output enable input (at OE Register).

Regarding claim 15, McClintock shows the dedicated inputs for I/O control comprise a clock enable input (ENA).

Regarding claim 17, McClintock shows the logic block array comprises a plurality of logic blocks.

Regarding claim 21, McClintock shows the interconnect matrix comprises a programmable interconnect matrix (programmably, col. 5, line 63).

Regarding claim 22, McClintock shows the interconnect matrix couples the memory block to one of the horizontal routing channels, one of the vertical routing channels, and the logic block array (col. 5 & 6)

Regarding claims 23-25, McClintock teaches that a programmable logic device can be any desired size (col. 5, lines 55).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 6-7, 9-11, 13-15, 17-27, and 29-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Cliff et al (5,689,195).

Regarding claim 1, Cliff shows a programmable logic device (Fig. 1) comprising:

One or more horizontal routing channels (60);

One or more vertical routing channels (80 or 80');

One or more logic elements (half row of 20s is one logic element) each configured to connect between one of the horizontal routing channels and one of the vertical routing channels, wherein each of the logic elements comprises (i) a logic block array (one LAB including 2 blocks, 4 logic modues, 30, is considered one block), and (ii) an interconnect matrix (70) coupled to the logic block array, the horizontal routing channel and the vertical routing channel; and

A memory block (40) coupled to either (a) the interconnect matrix (70, Fig. 2) or (b) the horizontal routing channel (60) and the vertical routing channel (80').

Regarding claim 2, Cliff shows the memory block comprises a first port (454 and 456) connected to one of the horizontal routing channels and a second port (452) connected to one of the vertical routing channels.

Regarding claim 6, Cliff shows the memory block is coupled to the interconnect matrix (70 connected to memory, Fig. 7)

Regarding claim 7, Cliff shows a plurality of I/O blocks, wherein each I/O block of the plurality of I/O blocks is connected to a different end of the horizontal (140) and the vertical routing channels (160).

Regarding claims 9 &10, Cliff shows one or more dedicated inputs for I/O cell control (180, Fig. 4).

Regarding claim 11, Cliff shows one or more dedicated clocks inputs (200, Fig. 4).

Regarding claim 13, Cliff shows the dedicated inputs for I/O control comprise a reset input (662, Fig. 9).

Regarding claim 14, Cliff shows the dedicated inputs for I/O control comprise an output enable input (692, Fig. 9).

Regarding claim 15, Cliff shows the dedicated inputs for I/O control comprise an output enable input (180).

Regarding claim 17, Cliff shows the logic block array comprises a plurality of logic blocks.

Regarding claim 18, Cliff shows each logic block of the logic block array comprises a product term array (92, Fig. 3 and col.7, lines 12-18) configured to receive inputs from the interconnect matrix.

Regarding claim 19, Cliff shows each of the logic blocks further comprise a plurality of macrocells (34, Fig. 3) each having an output coupled to the interconnect matrix.

Regarding claim 20, Cliff shows each of the logic blocks further comprises an OR array (32 or ULB, can be configured as any logic gate, col. 5) coupling the product term array to the plurality of macrocells.

Regarding claim 21, Cliff shows the interconnect matrix comprises a programmable interconnect matrix.

Regarding claims 23, Cliff shows a plurality of horizontal routing channels and a plurality of vertical routing channels (Fig. 1).

Regarding claim 24-25, Cliff shows at least four logic elements (each half row is considered one logic element, Fig. 1).

Regarding claim 26, Cliff shows a programmable logic device comprising:

A plurality of horizontal routing channels (60);

A plurality of vertical routing channels (80 and 80');

A plurality of first memory blocks (2 memory block '40' from two rows start from top row); and

A plurality of logic block arrays (first two half row of 20s), wherein each of the plurality of first memory blocks and each of the plurality of logic block arrays is coupled

between one of the plurality of horizontal routing channels (60 top) and one of the plurality of vertical routing channels (80').

Claims 27, & 29-32, the limitations are describes above and Cliff teaches that the LE and logic block arrays size can be expands to any desire size.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 3-5, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff '195 in view of Veenstra (5,977,791).

Cliff shows the claimed invention except for the memory block is configured as a synchronous dual port memory or as an asynchronous dual port memory or as a synchronous FIFO.

However, in figures 7-9 of Veenstra shows the memory block is configured as an synchronous dual port memory or as an asynchronous dual port memory or as a synchronous FIFO.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the memory block (Fig. 7-9) of Veenstra in place of the memory block of Cliff (40) in order to enhanced the logic functions.

3. Claims 12 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff'195 in view of Jefferson et al (6,130,552).

Cliff shows the claimed invention except for a phase lock loop circuit configured to generate one or more global clock signals in response to one or more input clock signals.

However, Jefferson shows a phase lock loop circuit (Fig. 5 & 6) configured to generate one or more global clock signals (GCLK) in response to one (300) or more input clock signals.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a phase lock loop circuit (Fig. 5 & 6) of Jefferson in the programmable logic device in order to reduces or minimizes clock skew when distributing a clock signal within the integrated circuit.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 703-306-4507. The examiner can normally be reached on M-F (8:00-5:30) second Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Anh Tran
October 9, 2001

Michael J. Tokar

Michael Tokar
Supervisory Patent Examiner
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